

Validation and Testing of Design Hardening for Single Event Effects Using the 8051 Microcontroller

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Abstract - With the dearth of dedicated radiation hardened foundries, new and novel techniques are being developed for hardening designs using non-dedicated foundry services. In this paper, we will discuss the implications of validating these methods for the single event effects (SEE) in the space environment. Topics include the types of tests that are required and the design coverage (i.e., design libraries: do they need validating for each application?). Finally, an 8051 microcontroller core from NASA Institute of Advanced Microelectronics (IA μ E) CMOS Ultra Low Power Radiation Tolerant (CULPRIT) design is evaluated for SEE mitigative techniques against two commercial 8051 devices.

Index Terms – Single Event Effects, Hardened-By-Design, microcontroller, radiation effects.

I. INTRODUCTION

NASA constantly strives to provide the best capture of science while operating in a space radiation environment using a minimum of resources [1,2]. With a relatively limited selection of radiation-hardened microelectronic devices that are often two or more generations of performance behind commercial state-of-the-art technologies, NASA's performance of this task is quite challenging. One method of alleviating this is by the use of commercial foundry alternatives with no or minimally invasive design techniques for hardening. This is often called hardened-by-design (HBD). Building custom-type HBD devices using design libraries and automated design tools may provide

NASA the solution it needs to meet stringent science performance specifications in a timely, cost-effective, and reliable manner.

However, one question still exists: traditional radiation-hardened devices have lot and/or wafer radiation qualification tests performed; what types of tests are required for HBD validation?

II. TESTING HBD DEVICES CONSIDERATIONS

Test methodologies in the United States exist to qualify individual devices through standards and organizations such as ASTM, JEDEC, and MIL-STD-883. Typically, TID (Co-60) and SEE (heavy ion and/or proton) are required for device validation. So what is unique to HBD devices?

As opposed to a "regular" commercial-off-the-shelf (COTS) device or application specific integrated circuit (ASIC) where no hardening has been performed, one needs to determine how validated is the design library as opposed to determining the device hardness. That is, by using test chips, can we "qualify" a future device using the same library?

Consider if Vendor A has designed a new HBD library portable to foundries B and C. A test chip is designed, tested, and deemed acceptable. Nine months later a NASA flight project enters the mix by designing a new device using Vendor A's library. Does this device require complete radiation qualification testing? To answer this, other questions must be asked.

How complete was the test chip? Was there sufficient statistical coverage of all library elements to validate each cell? If the new NASA design uses a partially or insufficiently characterized portion of the design library, full testing might be required. Of course, if part of the HBD was relying on inherent radiation hardness of a process, some of the tests (like SEL in the earlier example) may be waived.

Other considerations include speed of operation and operating voltage. For example, if the test chip was

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tested statically for SEE at a power supply voltage of 3.3V, is the data applicable to a 100 MHz operating frequency at 2.5V? Dynamic considerations (i.e., non-static operation) include the propagated effects of Single Event Transients (SETs). These can be a greater concern at higher frequencies.

The point of the considerations is that the design library must be known, the coverage used during testing is known, the test application must be thoroughly understood and the characteristics of the foundry must be known. If all these are applicable or have been validated by the test chip, then no testing may be necessary. A task within NASA's Electronic Parts and Packaging (NEPP) Program was performed to explore these types of considerations.

III. HBD TECHNOLOGY EVALUATION USING THE 8051 MICROCONTROLLER

With their increasing capabilities and lower power consumption, microcontrollers are increasingly being used in NASA and DOD system designs. There are existing NASA and DoD programs that are doing technology development to provide HBD. Microcontrollers are one such vehicle that is being investigated to quantify the radiation hardness improvement. Examples of these programs are the 8051 microcontroller being developed by Mission Research Corporation (MRC) and the IA μ E (the focus of this study). As these HBD technologies become available, validation of the technology, in the natural space radiation environment, for NASA's use in spaceflight systems is required.

The 8051 microcontroller is an industry standard architecture that has broad acceptance, wide-ranging applications and development tools available. There are numerous commercial vendors that supply this controller or have it integrated into some type of system-on-a-chip structure. Both MRC and IA μ E chose this device to demonstrate two distinctly different technologies for hardening. The MRC example of this is to use temporal latches that require specific timing to ensure that single event effects are minimized. The IA μ E technology uses ultra low power, and layout and architecture HBD design rules to achieve their results. These are fundamentally different than the approach by Aeroflex-United Technologies Microelectronics Center (UTMC), the commercial vendor of a radiation-hardened 8051, that built their 8051 microcontroller using radiation hardened processes. This broad range of technology within one device structure makes the 8051

an ideal vehicle for performing this technology evaluation.

The objective of this work is the technology evaluation of the CULPRiT process [3] from IA μ E. The process has been baselined against two other processes, the standard 8051 commercial device from Intel and a version using state-of-the-art processing from Dallas Semiconductor. By performing this side-by-side comparison, the cost benefit, performance, and reliability trade study can be done.

In the performance of the technology evaluation, this task developed hardware and software for testing microcontrollers. A thorough process was done to optimize the test process to obtain as complete an evaluation as possible. This included taking advantage of the available hardware and writing software that exercised the microcontroller such that all substructures of the processor were evaluated. This process is also leading to a more complete understanding of how to test complex structures, such as microcontrollers, and how to more efficiently test these structures in the future.

IV. TEST DEVICES

Three devices were used in this test evaluation. The first is the NASA CULPRiT device, which is the primary device to be evaluated. The other two devices are two versions of a commercial 8051, manufactured by Intel and Dallas Semiconductor, respectively.

The Intel devices are the ROMless, CMOS version of the classic 8052 MCS-51 microcontroller. They are rated for operation at +5V, over a temperature range of 0 to 70 °C and at a clock speeds of 3.5 MHz to 24 MHz. They are manufactured in Intel's P629.0 CHMOS III-E process.

The Dallas Semiconductor devices are similar in that they are ROMless 8052 microcontrollers, but they are enhanced in various ways. They are rated for operation from 4.25 to 5.5 Volts over 0 to 70 °C at clock speeds up to 25 MHz. They have a second full serial port built in, seven additional interrupts, a watchdog timer, a power fail reset, dual data pointers and variable speed peripheral access. In addition, the core is redesigned so that the machine cycle is shortened for most instructions, resulting in an effective processing ability that is roughly 2.5 times greater (faster) than the standard 8052 device. None of these features, other than those inherent in the device operation, were utilized in order to maximize the similarity between the Dallas and Intel test codes.

The CULPRiT technology device is a version of the

MSC-51 family compatible C8051 HDL core licensed from the Ultra Low Power (ULP) process foundry. The CULPRiT technology C8051 device is designed to operate at a supply voltage of 500 mV and includes an on-chip input/output signal level-shifting interface with conventional higher voltage parts. The CULPRiT C8051 device requires two separate supply voltages; the 500 mV and the desired interface voltage. The CULPRiT C8051 is ROMless and is intended to be instruction set compatible with the MSC-51 family.

V. TEST HARDWARE

The 8051 Device Under Test (DUT) was tested as a component of a functional computer as illustrated in Figure 1. Aside from DUT itself, the other components of the DUT computer were removed from the immediate area of the irradiation beam. A small card (one per DUT package type) with a unique hard-wired identifier byte contained the DUT, its crystal, and bypass capacitors (and voltage level shifters for the CULPRiT DUTs). This "DUT Board" was connected to the "Main Board" by a short 60-conductor ribbon cable. The Main Board had all other components required to complete the DUT Computer, including some which nominally are not necessary in some designs (such as external RAM, external ROM and address latch).

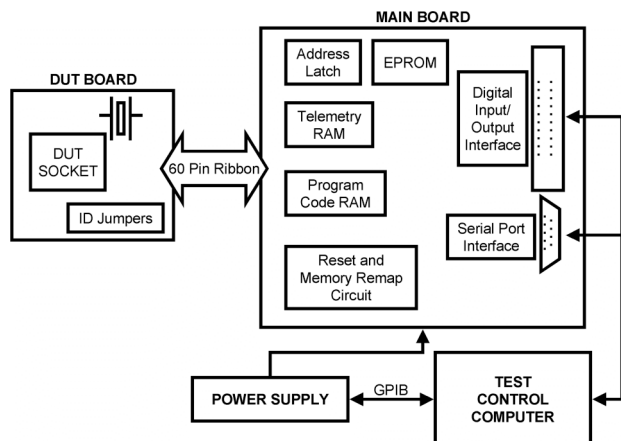


Figure 1. Hardware Block Diagram of the Test System.

The DUT Computer and the Test Control Computer were connected via a serial cable and communications were established between the two by the Controller (that runs custom designed serial interface software). This Controller software allowed for commanding of the DUT, downloading DUT Code to the DUT, and real-time error collection from the DUT during and post

irradiation. A 1 Hz signal source provided an external watchdog timing signal to the DUT, whose watchdog output was monitored via an oscilloscope. The power supply was monitored to provide indication of latchup.

VI. TEST SOFTWARE

The 8051 test software concept is straightforward. It was designed to be a modular series of small test programs each exercising a specific part of the DUT (Figure 2). Since each test was stand alone, they were loaded independently of each other for execution on the DUT. This ensured that only the desired portion of the 8051 DUT was exercised during the test and helped pinpoint location of errors that occur during testing. All test programs resided on the controller PC until loaded via the serial interface to the DUT computer. In this way, individual tests could have been modified at any time without the necessity of burning PROMs. Additional tests could have also been developed and added without impacting the overall test design. The only permanent code, which was resident on the DUT, was the boot code and serial code loader routines that established communications between the controller PC and the DUT.

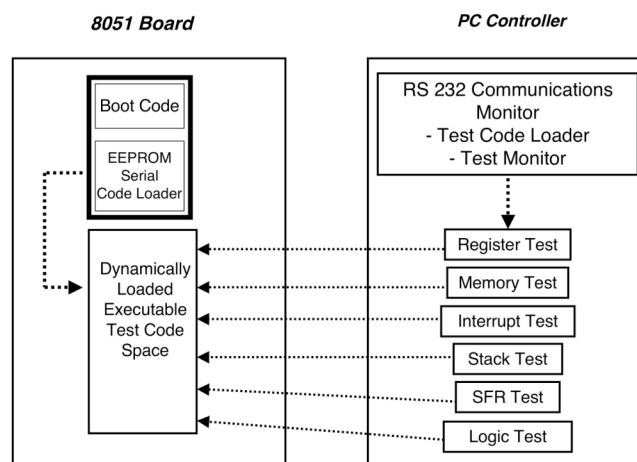


Figure 2. Test Software Block Diagram.

All test programs implemented:

- An external Universal Asynchronous Receive and Transmit device (UART) for transmission of error information and communication to controller computer.
- An external real-time clock for data error tag.
- A watchdog routine designed to provide visual verification of 8051 health and restart test code if necessary.
- A "foul-up" routine to reset program counter if

it wanders out of code space.

- An external telemetry data storage memory to provide backup of data in the event of an interruption in data transmission.

The brief description of each of the software tests used is given below. It should be noted that for each test, the returned telemetry (including time tag) was sent to both the test controller and the telemetry memory, giving the highest reliability that all data is captured.

Interrupt – This test used 4 of 6 available interrupt vectors (Serial, External, Timer0 Overflow, and Timer1 Overflow) to trigger routines that sequentially modified a value in the accumulator which was periodically compared to a known value. Unexpected values were transmitted with register information.

Logic – This test performed a series of logic and math computations and provided three types of error identifications: 1) addition/subtraction, 2) logic and 3) multiplication/division. All miscompares of computations and expected results were transmitted with other relevant register information.

Memory – This test loaded internal data memory at locations D:0x20 through D:0xff (or D:0x20 through D:0x080 for the CULPRiT DUT), indirectly, with an 0x55 pattern. Compares were performed continuously and miscompares were corrected while error information and register values were transmitted.

Program Counter - The program counter was used to continuously fetch constants at various offsets in the code. Constants were compared with known values and miscompares were transmitted along with relevant register information.

Registers – This test loaded each of four (0,1,2,3) banks of general-purpose registers with either 0xAA (for banks 0 and 2) or 0x55 (for banks 1 and 3). The pattern was alternated in order to test the Program Status Word (PSW) special function register, which controls general-purpose register bank selection. General-purpose register banks were then compared with their expected values. All miscompares were corrected and error information was transmitted.

Special Function Registers (SFR) – This test used learned static values of 12 out of 21 available SFRs and then constantly compared the learned value with the current one. Miscompares were reloaded with learned value and error information was transmitted.

Stack – This test performed arithmetic by pushing and popping operands on the stack. Unexpected results were attributed to errors on the stack or to the stack pointer

itself and were transmitted with relevant register information.

VII. TEST METHODOLOGY

The DUT Computer booted by executing the instruction code located at address 0x0000. Initially, the device at this location was an EPROM previously loaded with "Boot/Serial Loader" code. This code initialized the DUT Computer and interface through a serial connection to the controlling computer, the "Test Controller". The DUT Computer downloaded Test Code and put it into Program Code RAM (located on the Main Board of the DUT Computer). It then activated a circuit which simultaneously performed two functions: held the DUT reset line active for some time (~10 ms); and, remapped the Test Code residing in the Program Code RAM to locate it to address 0x0000 (the EPROM will no longer be accessible in the DUT Computer's memory space). Upon awaking from the reset, the DUT computer again booted by executing the instruction code at address 0x0000, except this time that code was not be the Boot/Serial Loader code but the Test Code.

The Test Control Computer always retained the ability to force the reset/remap function, regardless of the DUT Computer's functionality. Thus, if the test ran without a Single Event Functional Interrupt (SEFI) either the DUT Computer itself or the Test Controller could have terminated the test and allowed the post-test functions to be executed. If a SEFI occurred, the Test Controller forced a reboot into Boot/Serial Loader code and then executed the post-test functions.

During any test of the DUT, the DUT exercised a portion of its functionality (e.g., Register operations or Internal RAM check, or Timer operations) at the highest utilization possible, while making a minimal periodic report to the Test Control Computer to convey that the DUT Computer was still functional. If this report ceased, the Test Controller knew that a SEFI had occurred. This periodic data was called "telemetry". If the DUT encountered an error that was not interrupting the functionality (e.g., a data register miscompare) it sent a more lengthy report through the serial port describing that error, and continued with the test.

VIII. TEST RESULTS

All testing reported in this summary was conducted at the Texas A&M University Cyclotron Facility using the 15 MeV/amu energy tune. Effective Linear Energy Transfer (LET) for the testing ranged from 2 to 85 MeV-cm²/mg.

Figures 3 through 9 show the per-bit cross section curves for the seven different software tests. In each of these figures, the cross section curves for the Intel, Dallas Semiconductor and CULPRiT devices are plotted for comparison. Note: a data point plotted with a downward pointing arrow indicates that no events were observed for that condition and the point is just plotted at the one over the total fluence level.

The first observation to make from these figures is the difference in the LET threshold levels between the commercial versions and the CULPRiT. In almost every case, the two commercial devices show events at the lowest LET tested to, approximately 2 MeV-cm²/mg. The CULPRiT devices, on the other hand, do not show any effects until an LET of greater than 20 MeV-cm²/mg.

In Figures 3 through 8, the saturation cross section for the commercial devices is typically one to two orders of magnitude higher than that of the CULPRiT devices. In Figure 9 (Memory Test results), the initial flow of the cross section curves seems to indicate that this trend will continue. However, after an LET of approximately 60 MeV-cm²/mg, the CULPRiT data takes an approximate one order of magnitude jump in cross section that is not observed in any of the other tests. The proposed mechanism for this observation is presented in the Discussion section to follow.

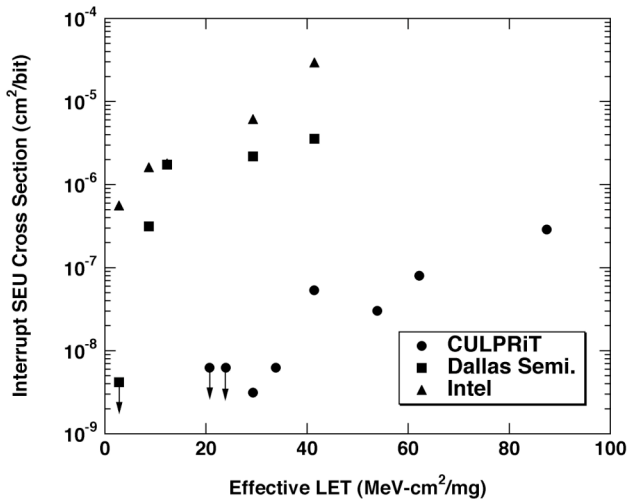


Figure 3. Interrupt Test Cross Section Comparison.

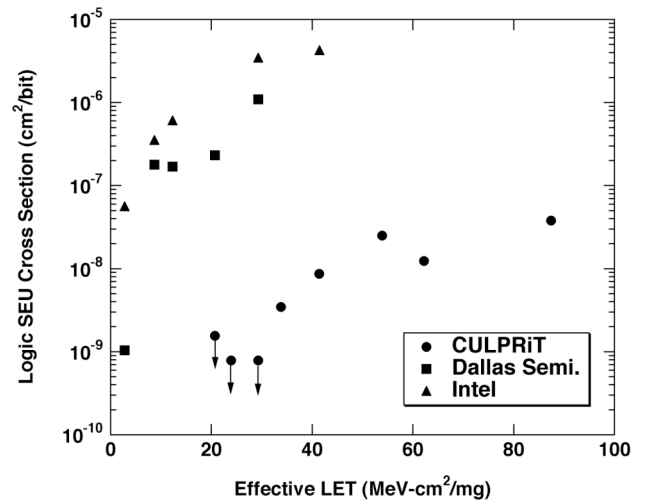


Figure 4. Logic Test Cross Section Comparison.

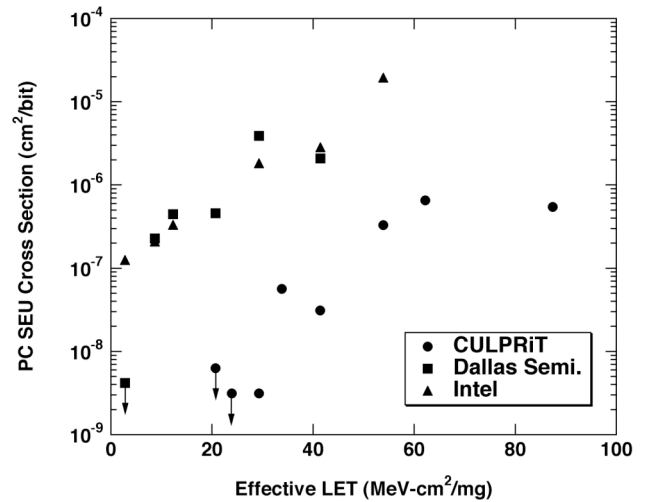


Figure 5. Program Counter Test Cross Section Comparison.

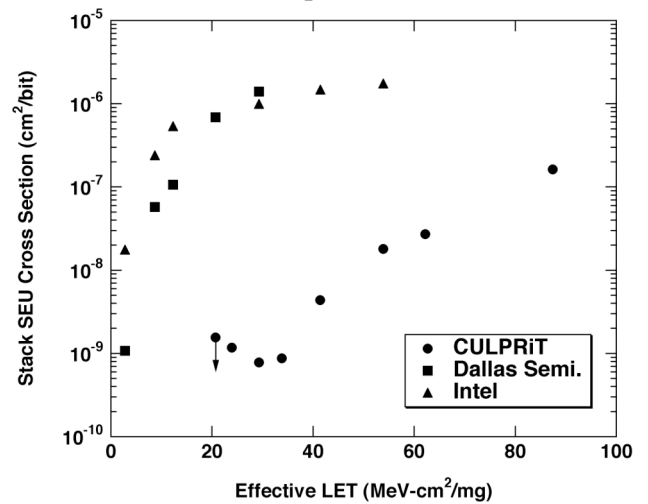


Figure 6. Stack Test Cross Section Comparison.

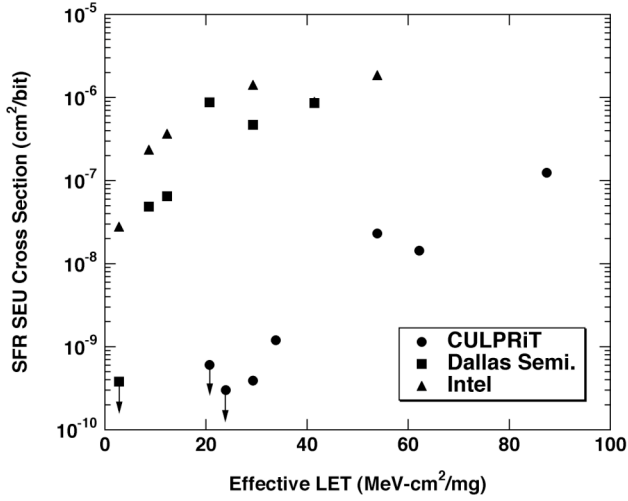


Figure 7. SFR Test Cross Section Comparison.

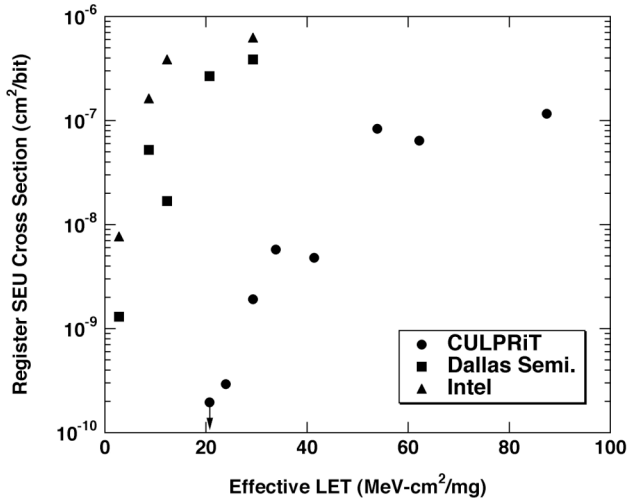


Figure 8. Register Test Cross Section Comparison.

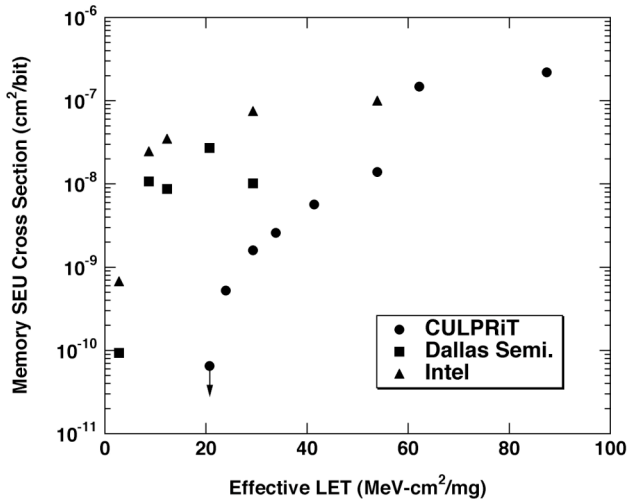


Figure 9. Memory Test Cross Section Comparison.

Finally, Figure 10 shows the SEFI cross section for all three devices tested (SEFI data is available since the microcontroller was actively tested). As with the SEU type events, the threshold LETs shown for the commercial devices is approximately 2 and the CULPRiT devices show thresholds above 20 MeV-cm²/mg. Also, the saturation cross section is over an order of magnitude lower for the CULPRiT technology than for the commercial technologies.

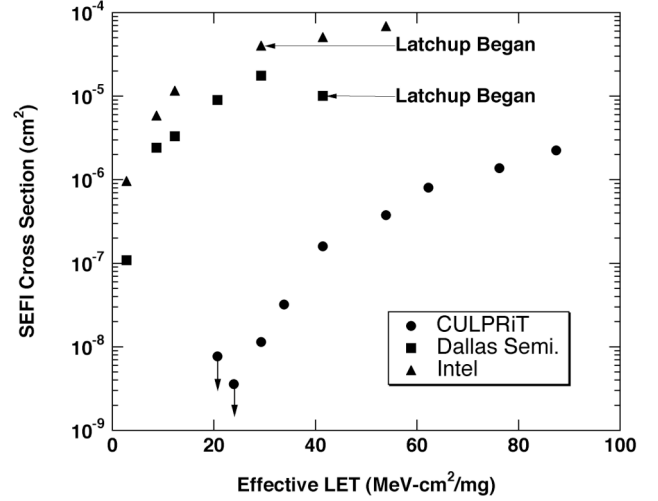


Figure 10. SEFI Cross Section Comparison.

Figure 10 also shows the LET values where latchup events started. Latchup for the Intel device occurs at an LET of approximately 30 MeV-cm²/mg and the Dallas Semiconductor device shows evidence of latchup around 40 MeV-cm²/mg. The CULPRiT technology devices do not show any evidence of latchup to the highest LET tested, approximately 85 MeV-cm²/mg. Since no latchup was observed for the CULPRiT devices, a measurement of latchup cross section for the commercial devices was not done (i.e., not required for the validation of the CULPRiT technology).

IX. DISCUSSION

A. Single Event Latchup

The main argument for why latchup is not an issue for the CULPRiT devices is that the operating voltage of 0.5 volts should be below the holding voltage required for latchup to occur. In addition to this, the cell library used also incorporates the heavy dual guard-barring scheme [4]. This scheme has been demonstrated multiple times to be very effective in rendering CMOS circuits completely immune to SEL up to test limits of 120 MeV-cm²/mg. This is true in circuits operating at 5,

3.3, and 2.5 Volts, as well as the 0.5 Volt CULPRiT circuits. In one case, a 5 Volt circuit fabricated on non-epi wafers even exhibited such SEL immunity.

The CULPRiT device design chose to continue to pay the real estate cost of the guard bars (~10-15%) even considering the 0.5 Volt circuits. With the applied back bias voltages considered, however, there are voltages exceeding holding voltage present.

B. Single Event Upset

The primary structure of the storage unit used in the CULPRiT devices is the Single Event Resistant Topology (SERT) [5]. Given the SERT cell topology and a single upset node assumption, it is expected that the SERT cell will be completely immune to SEUs occurring internal to the memory cell itself. Obviously there are other things going on. The CULPRiT 8051 results reported here are quite similar to some results obtained with a CULPRiT CCSDS lossless compression chip (USES) [6]. The CULPRiT USES was synthesized using exactly the same tools and library as the CULPRiT 8051.

With the CULPRiT USES, the SEU cross section data [7] was taken as a function of frequency at two LET values, 37.6 and 58.5 MeV-cm²/mg. In both cases the data fit well to a linear model where cross section is proportional to clock. In the LET 37.6 case, the zero frequency intercept occurred essentially at the zero cross section point, indicating that virtually all of these SEUs are captured SETs from the combinational logic. The LET 58.5 data indicated that the SET (frequency dependent) component is sitting on top of a "dc-bias" component – presumably a second upset mechanism is occurring internal to the SERT cells only at a second, higher LET threshold.

The SET mitigation scheme used in the CULPRiT devices is based on the SERT cell's fault tolerant input property when redundant input data is provided to separate storage nodes. The idea is that the redundant input data is provided through a total duplication of combinational logic (referred to as "dual rail design") such that a simple SET on one rail cannot produce an upset. Therefore, some other upset mechanism must be happening. It is possible that a single particle strike is placing an SET on both halves of the logic streams, allowing an SET to produce an upset. Care was taken to separate the dual sensitive nodes in the SERT cell layouts but the automated place-and-route of the combinational logic paths may have placed dual sensitive nodes close enough.

At this point, the theory for the CULPRiT SEU response is that at about an LET of 20, the energy deposition is sufficiently wide enough (and in the right locations) to produce an SET in both halves of the combinational logic streams. Increasing LET allows for more regions to be sensitive to this effect, yielding a larger cross section. Further, the second SEU mechanism that starts at an LET of about 40-60 has to do with when the charge collection disturbance cloud gets large enough to effectively upset multiples of the redundant storage nodes within the SERT cell itself. In this 0.35 μm library, the node separation is several microns. However, since it takes less charge to upset a node operating at 0.5 Volts, with transistors having effective thresholds around 70 mV, this is likely the effect being observed. Also the fact that the per-bit memory upset cross section for the CULPRiT devices and the commercial technologies are approximately equal, as shown in Figure 9, indicates that the cell itself has become sensitive to upset.

X. SUMMARY

A detailed comparison of the SEE sensitivity of a HBD technology (CULPRiT) utilizing the 8051 microcontroller as a test vehicle has been completed. This paper discusses the test methodology used and presents a comparison of the commercial versus CULPRiT technologies based on the data taken. The CULPRiT devices consistently show significantly higher threshold LETs and an immunity to latchup. In all but the memory test at the highest LETs, the cross section curves for all upset events is one to two orders of magnitude lower than the commercial devices. Additionally, theory is presented, based on the CULPRiT technology, that explain these results.

This paper also demonstrates the test methodology for quantifying the level of hardness designed into a HBD technology. By using the HBD technology in a real-world device structure (i.e., not just a test chip), and comparing results to equivalent commercial devices, one can have confidence in the level of hardness that would be available from that HBD technology in any circuit application.

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